AMENDMENTS TO THE CLAIMS

Claim 1 (Currently Amended) A ferroelectric memory device comprising a plurality of memory cells, each memory cell of the plurality of memory cells including a respective memory cell transistor and a respective memory cell capacitor, and the plurality of memory cells being arranged in a matrix along a first direction and along a second direction that is perpendicular to the first direction ~~such that the ferroelectric memory device includes a plurality of memory cell transistors and a plurality of memory cell capacitors~~,

wherein each respective memory cell capacitor of the plurality of memory cells comprises:

a lower electrode connected to a bit line via the respective memory cell transistor;

a ferroelectric layer formed on an upper surface of the lower electrode and having a width direction that is the same as a width direction of the lower electrode; and

an upper electrode formed on an upper surface of the ferroelectric layer and having a width direction that is the same as the width direction of the lower electrode,

wherein the lower electrode ~~electrodes~~ of each respective ~~the~~ memory cell capacitor is ~~capacitors are~~ independent from the lower electrodes of other memory cell capacitors, such that each respective memory cell capacitor includes a separate lower electrode ~~one another~~,

wherein each respective ~~the~~ upper electrode ~~electrodes~~ of each respective ~~the~~ memory cell capacitor of the plurality of memory cells that are only arranged along the second direction forms ~~capacitors form~~ a continuous plate electrode covering only the respective independent lower electrodes of each respective memory cell capacitor of the plurality of memory cells that are only arranged along the second direction ~~cell capacitors~~, and

wherein the width of each respective upper electrode in the first direction is narrower

than the width of each respective ferroelectric layer in the first direction.

Claim 2 (Currently Amended) The ferroelectric memory device as defined in Claim 1 wherein the width of each respective independent lower electrode in the first direction is narrower than the width of each respective ferroelectric layer in the first direction.

Claim 3 (Currently Amended) The ferroelectric memory device as defined in Claim 2

wherein the width of each respective upper electrode in the first direction and the width of each respective independent lower electrode in the first direction are substantially the same, and

wherein a position of both edges along the second direction of each respective upper electrode ~~in the width direction~~ and a position of both edges along the second direction of each respective independent lower electrode ~~in the width direction~~ are substantially the same ~~aligned~~.

Claim 4 (Currently Amended) The ferroelectric memory device as defined in Claim 2

wherein the width of each respective upper electrode in the first direction and the width of each respective independent lower electrode in the first direction are substantially the same, and

wherein a position of both edges along the second direction of each respective upper electrode ~~in the width direction~~ and a position of both edges along the second direction of each respective independent lower electrode ~~in the width direction~~ are different from each other.

Claim 5 (Currently Amended) A ferroelectric memory device comprising a plurality of

memory cells, each memory cell of the plurality of memory cells including a respective memory cell transistor and a respective memory cell capacitor, and the plurality of memory cells being arranged in a matrix along a first direction and along a second direction that is perpendicular to the first direction ~~such that the ferroelectric memory device includes a plurality of memory cell transistors and a plurality of memory cell capacitors~~,

wherein each respective memory cell capacitor of the plurality of memory cells comprises:

a lower electrode connected to a bit line via the respective memory cell transistor;

a ferroelectric layer formed on an upper surface of the lower electrode; and

an upper electrode formed on an upper surface of the ferroelectric layer,

wherein the lower electrode ~~electrodes~~ of each respective ~~the~~ memory cell capacitor is ~~capacitors are~~ independent from the lower electrodes of other memory cell capacitors, such that each respective memory cell capacitor includes a separate lower electrode ~~one another~~,

wherein each respective ~~the~~ upper electrode ~~electrodes~~ of each respective ~~the~~ memory cell capacitor of the plurality of memory cells that are only arranged along the second direction forms ~~capacitors form~~ a continuous plate electrode covering only the respective independent lower electrodes of each respective memory cell capacitor of the plurality of memory cells that are only arranged along the second direction ~~cell capacitors~~,

wherein a position of one edge along the second direction of each respective upper electrode substantially aligns with a position of one edge along the second direction of each respective ferroelectric layer, and

wherein another edge along the second direction of each respective upper electrode is inwardly located at a position relative to another edge along the second direction of each

respective ferroelectric layer.

Claim 6 (Currently Amended) The ferroelectric memory device as defined in Claim 5 wherein one edge along the second direction of each respective independent lower electrode is inwardly located at a position relative to one edge along the second direction of each respective upper electrode, and a position of another edge along the second direction of each respective independent lower electrode substantially aligns with a position of another edge along the second direction of each respective upper electrode.

Claim 7 (Currently Amended) A ferroelectric memory device comprising a plurality of memory cells, each memory cell of the plurality of memory cells including a respective memory cell transistor and a respective memory cell capacitor, and the plurality of memory cells being arranged in a matrix along a first direction and along a second direction that is perpendicular to the first direction ~~such that the ferroelectric memory device includes a plurality of memory cell transistors and a plurality of memory cell capacitors~~,

wherein each respective memory cell capacitor of the plurality of memory cells comprises:

a lower electrode connected to a bit line via the respective memory cell transistor;

a ferroelectric layer formed on an upper surface of the lower electrode; and

an upper electrode formed on an upper surface of the ferroelectric layer,

wherein the lower electrode ~~electrodes~~ of each respective ~~the~~ memory cell capacitor is ~~capacitors are~~ independent from the lower electrodes of other memory cell capacitors, such that each respective memory cell capacitor includes a separate lower electrode ~~one another~~,

wherein each respective ~~the~~ upper electrode ~~electrodes~~ of each respective ~~the~~ memory cell capacitor of the plurality of memory cells that are only arranged along the second direction forms ~~capacitors form~~ a continuous plate electrode covering only the respective independent lower electrodes of each respective memory cell capacitor of the plurality of memory cells that are only arranged along the second direction ~~cell capacitors~~,

wherein a position of one edge along the second direction of each respective upper electrode substantially aligns with a position of one edge along the second direction of each respective ferroelectric layer,

wherein another edge along the second direction of each respective upper electrode is inwardly located at a position relative to another edge along the second direction of each respective ferroelectric layer, and

wherein one edge along the second direction of each respective independent lower electrode is inwardly located at a position relative to one edge along the second direction of each respective ferroelectric layer, and a position of another edge along the second direction of each respective independent lower electrode substantially aligns with a position of another edge along the second position of each respective ferroelectric layer.

Claim 8 (Currently Amended) The ferroelectric memory device as defined in Claim 1 wherein each respective independent lower electrode includes a groove-type structure.

Claim 9 (Currently Amended) The ferroelectric memory device as defined in Claim 8 wherein a groove formed in each respective independent lower electrode extends along a direction that is parallel to a direction along which each respective upper electrode extends.

Claim 10 (Currently Amended) The ferroelectric memory device as defined in Claim 8 wherein a direction along which a groove formed in each respective independent lower electrode extends is perpendicular to a direction along which each respective upper electrode extends.

Claims 11-15 (Cancelled)